FORM PTO-1449/A and B (Modified)	APPLICATION NO.: 09/919,~~949~~ 495	ATTY. DOCKET NO.: S1022.80718US00
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE: July 30, 2001	CONFIRMATION NO.: 4927
	APPLICANT: Sebastien Ferroussat	
Sheet [ ] of [ ]	GROUP ART UNIT: 2193	EXAMINER: T.V. Mai

U.S. PATENT DOCUMENTS

Examiner's Initials	Cite No.	U.S. Patent Document Number	U.S. Patent Document Kind Code	Name of Patentee or Applicant of Cited Document	Date of Publication or of issue of Cited Document MM-DD-YYYY
Mmi		4,604,723		James L. .Burrows	08/05/86

FOREIGN PATENT DOCUMENTS

Examiner's Initials	Cite No.	Foreign Patent Document Office/ Country	Foreign Patent Document Number	Foreign Patent Document Kind Code	Name of Patentee or Applicant of Cited Document (not necessary)	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)

OTHER ART — NON PATENT LITERATURE DOCUMENTS

Examiner's Initials	Cite No	Include name of the author (in CAPITAL LETTERS) title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, relevant page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)	
Mmi		European Search Report from European Patent Application 00410092.1 filed August 1, 2000		
		Mayur Mehta et al. "High-Speed Multiplier Design Using Multi-Input Counter And Compressor Circuits" Proceedings of the Symposium on Computer Arithmetic, US, Los Alamitos, IEEE Comp. Soc. Press, vol. SYMP. 10, June 26, 1991, pages 43-50, XP000222157		
		Norio Ohkubo et al. "A 4.4 NS CMOS 54 X 54-B Multiplier Using Pass-Transistor Multiplexer" IEEE Journal of Solid-State Circuits, US, IEEE Inc., New York, vol. 30, no. 3, March 1, 1995, pages 251-256, XP000502811		

EXAMINER	DATE CONSIDERED
Mmi	3/13/06

#EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.